ABSTRACT OF THE DISCLOSURE

METHOD OF POWER CONSUMPTION REDUCTION IN CLOCKED CIRCUITS

A method and apparatus for reducing power consumption of a clocked circuit containing a plurality of latches is provided. A first latch, within the plurality of latches, is located which has more than a predetermined slack. The possibility of substituting an available second latch (requiring less power to operate) is then determined, subject to the constraint that the slack after substitution should still be positive, although it may be less than the predetermined number mentioned above. Where such a possibility is determined to exist, the first latch is then replaced with the available second latch.